LZ95D71 M

Timing Pulse Generator LSI for CCD

DESCRIPTION

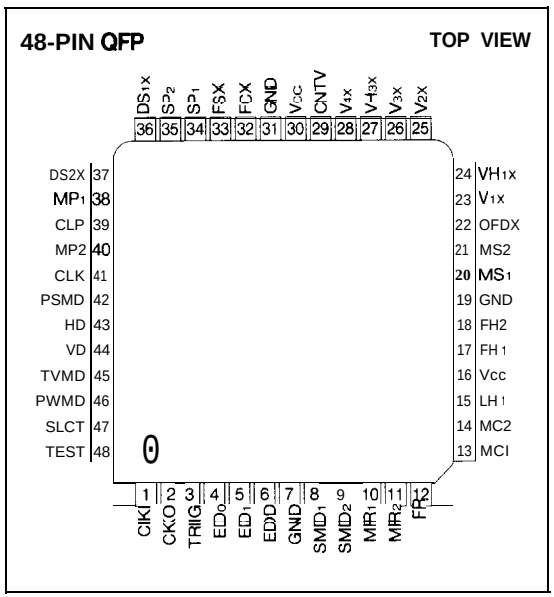
The LZ95D71 M is a CMOS timing generator LSI which provides timing pulses used to drive a CCD area sensor, in combination with the SSG LSI (LZ95D52/M).

FEATURES

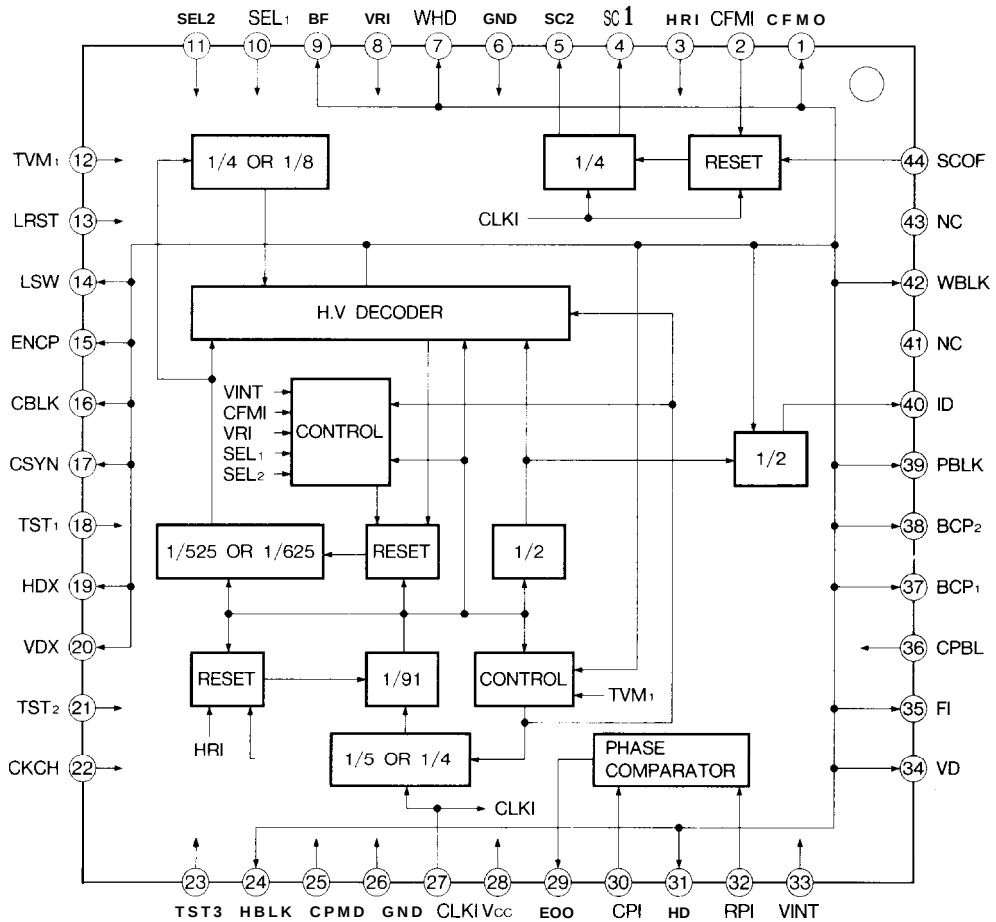
- Switchable between 410000 pixels CCD and 470000 pixels CCD
- Switchable between NTSC (EIA) and PAL (CCIR) systems
- . Internal electronic shutter :

  Shutter speed is selectable from 1 /60 (PAL : 1 /50), 1/1 25, 1 /250, 1 /500, 1/1 000, 1/2 000, 1/4 000 and 1/10 000 s, in addition to this, 1/100 s, (PAL : 1/120 s) in flicker -less mode using parallel code. Shutter speed can also be controlled in 1 H period using a serial code
- Single +5 V power supply
- . Package : 48-pin QFP(QFP048-P-0707)

PIN CONNECTIONS



BLOCK DIAGRAM



NOTE :

Pin numbers apply to the 44-pin QFP.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	Vcc	–0.3 to 7.0	V
Input voltage	VI	– 0.3 to Vcc +0.3	v
Output voltage	Vo	– 0.3 to Vcc + 0.3	v
Operation temperature	Topr	–20 to +70	℃
Storage temperature	Tstg	–55 to +150	"c

DC CHARACTERISTICS

(Vcc = +5 V±5%, Ta=–20 to +70℃)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input Low voltage	V_{IL}				1.5	v	1
Input High voltage	V_{IH}		3.5			v	
Input High threshold voltage	V_{T+}				3.7	v	2
Input Low threshold voltage	V_{T-}		1.0			V	
Hysteresis voltage	$V_{T+} - V_{T-}$		0.4			v	
Input Low current	I_{IL1}	VI=0 V			1.0	μA	3
	I_{IL2}	VI=o v	8.0		60	μA	4
Input High current	I_{IH1}	VI= Vcc			1.0	μA	5
	I_{IH2}	VI= Vcc	8.0		60	μA	6
Output High voltage	V_{OH1}	$I_{OH} = -2$ mA	4.0			v	7
Output High voltage	V_{OH2}	$I_{OH} = -6$ mA	4.0			v	8
Output Low voltage	V_{OL1}	$I_{OL} = 4$ mA			0.4	v	7
Output Low voltage	V_{OL2}	$I_{OL} = 12$ mA			0.4	v	8
Leak output current	$\|I_{OZ}\|$	High-Z			1.0	μA	

NOTE :

1. Applied to inputs (IC, ICO, ICU).
2. Applied to schmitt-trigger input (ICSU).
3. Applied to inputs (IC, ICD).
4. Applied to inputs (ICU, ICSU).
5. Applied to inputs (IC, ICU, ICSU).
6. Applied to input (ICD).
7. Applied to all outputs (0).
8. Applied to tri-state output (TO).

PIN FUNCTION (Pin numbers apply to 44-pin QFP)

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
1	CFMO	o	⎍	Color frame output	A pulse to control color frame; Occurs at every 4 fields in NTSC mode, occurs at every 8 fields in PAL mode.
2	CFMI	ICD	–	Color frame reset input	An input pin for color frame signal; Connect to external color frame signal in External Synchronous rode. Connect to CFMO (pin 1) in Internal Synchronous mode or Initialize mode with VINT (pin 33).
3	HRI	ICSU	–	Horizontal reset input	An input pin for resetting internal horizontal counter. Set open or to H level when not resetting.
4	SC_1	0	⎍⎍	Subcarrier output 1	An output pin for color subcarrier in NTSC mode. The frequency of the signal is 1/4 the CLKI (pin 27) frequency, The signal is reset by color frame pulse CFMI (pin 2). When the SCOF (pin 44) is H level or in PAL mode, it is held at L level.
5	SC2	o	⎍⎍	Subcarrier output 2	An output pin for color subcarrier in NTSC mode. When the phase of SC I (pin 4) is 180 degree, the phase of SC_2 is 90 degree in NTSC rode. When the SCOF (pin 44) is H level or in PAL mode, it is held at L level.
6	GND	–	·	Ground	A grounding pin.
7	WHD	0	⎍	Wide Horizontal drive pulse	An output pin for wide Horizontal drive pulse. The pulse width is equal to that of PBLK (pin 39) and the repetition is horizontal frequency.
8	VRI	ICSU	–	Vertical reset input	An input pin for resetting internal vertical counter. The input pulse is necessary 1/2 horizontal max. delay from vertical synchronous start point, because VRI is counted by 2 times horizontal frequency. Set open or to H level when not resetting.
9	BF	0	⎍ or ⎎	Burst flag	A pulse to define burst period, When CKCH (pin 22) is L level, the polarity is positive, and when CKCH is H level, the polarity is negative.
10	SELI	ICD	–	Non-interlace mode select 1	These inputs pin to select Interlace mode or Non-interlace mode, at Internal Synchronous mode. And in Non-interlace mode, switchable TV lines.
11	SEL2	ICD	–	Non-interlace mode select 2	

SELI	L	H	L	H
SEL2	L	L	H	H
TV mode	Interlace	Non-interlace		
NTSC	262.5H	260H	261 H	262H
PAL	312.5H	31 0H	311H	312H

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
12	TVM 1	ICD	–	TV mode select	An input pin to select TV standards. TVM1: L = TV mode NTSC; H = PAL
13	LRST	ICU	–	Line switch reset	The input resets the output from LSW (pin 14), Set open or to H level when not used.
14	LSW	0	⎍	Line switch	The signal switches between H and L at every line in PAL mode, It is set at Low level at the Ist line of the Ist field.
15	ENCP	0	⎍	Encoder DC clamp pulse	A clamp pulse that is used for recovering DC level. The repetition is horizontal frequency. When CKCH (Pin 22) is H level, the phase is change,
16	CBLK	0	n or u	Composite blanking pulse	Composite blanking pulses. In NTSC mode; H : 10.97 μs, V : 20 H period In PAL mode; H : 12.12 μs, V : 25 H period When CKCH (pin 23) is L level, the polarity is positive, and when CKCH is H level, the polarity is negative.
17	CSYN	0	u	Composite syncronus signal	A composite synchronous signal that comforms to RS-I 70 in NTSC mode and to CCIR in PAL mode.
18	TST1	ICD	–	Test terminal 1	A pin for tests. Set open or to L level in the Normal mode.
19	HDX	0	u	Horizontal drive pulse2	The pulse occurs at the start of lines and invert pulse of HD (pin 31). When LZ95D71 M is used for timing LSI, connect to HDI of timing LSI.
20	VDX	0	⎍	V drive pulse 2	The pulse occurs at the start of every field and invert pulse of VD (pin 34). When LZ95D71 M is used for timing LSI, connect to VDI of timing LSI.
21	TST2	ICD	–	Test terminal 2	A pin for tests. Set open or to L level in the Normal mode.
22	CKCH	ICD	–	Clock polarity select	An input pin to select main clock polariy. When LZ95D42/M is used for timing LSI, set to L level, and LZ95D71 M is used, set to H level. The polarity of CBLK (pin 16), PBLK (pin 39), BF (pin 9) end WBLK (pin 42) change, and the phase of ENCP (pin 15) and HBLK (pin 24) change with input level.
23	TST3	ICD	–	Test terminal 3	A pin for tests. Set open or to L level in the Normal mode.
24	HBLK	0	⎍	Horizontal blanking pulse	When CKCH (pin 22) is L level, pulse that correspondes to the cease period of the horizontal transfer pulse. When CKCH is H level, pulse is gate pulse of burst-flag.

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
25	CPMD	ICU	–	Clamp Pulse mode select	An input pin to stop or to continue BCPI (pin 37) and BCP2 (pin 38) pulses within the vertical blanking period, L level : continuous output. Open or H level : becomes Low level during the absence of effective pixels within V blanking period.
26	GND	–	–	Ground	A grounding pin.
27	CLKI	IC	⎍⎍	Main clock	An input pin for reference clock. Connect to timing LSI : Following frequencies appear on this pin; At NTSC mode :14.31818 MHz when TVMI = L level At PAL mode :14.1875 MHz when TVM1 = H level
28	Vcc	–	–	Power supply	Supply +5 V power.
29	EOO	TO	–	Phase comparator output	Phase comparator output for input signals RPI (pin 32) and CPI (pin 30). When CPI is advanced, output is Low level, When CPI is delayed, output is High level, When phases are equal, the terminal impedance is High.
30	CPI	ICD	–	Horizontal comparison input	An input pin for comparison signal to the phase comparator. Set open or to L level when comparator is not used.
31	HD	o	⎍	Horizontal drive pulse	The pulse occurs at the start of lines. When LZ95D42/M is used for timing LSI, connect to HDI of timing LSI.
32	RPI	ICD	–	Horizontal reference input	An input pin for the reference signal to the phase comparator. Set open or to L level when comparator is not used.
33	VINT	Icsu	–	Initialize input	An input pin for initializing circuit. It can be used field-reset input, and the circuit is initialized with the 1/2 dividing pulse of VI NT. The frequency of VINT is 60 Hz (NTSC) or 50 Hz (PAL). Set open or to H level when Internal Synchronization mode or no initializing
34	VD	o	n	V drive pulse	The pulse occurs at the start of every field. When LZ95D42/M is used for timing LSI, connect to VDI of timing LSI.
35	FI	o	n	Field index	The pulse is used for detecting field. At NTSC mode : ODD field; LOW EVEN field; HIGH At PAL mode : 1st and 3rd field; LOW 2nd and 4th field; HIGH

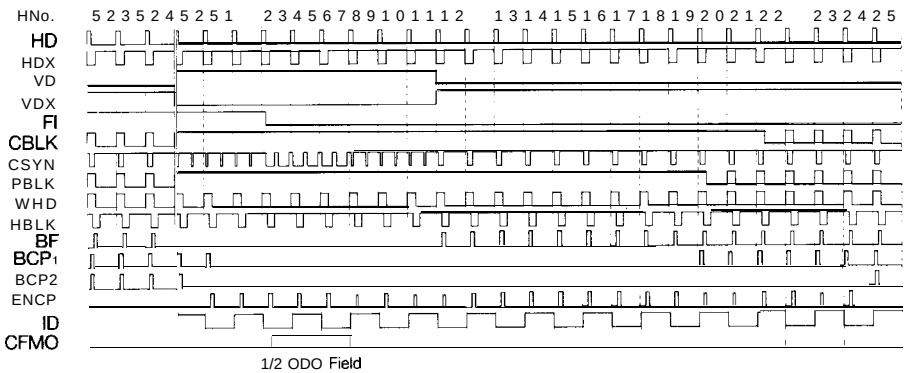
PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
36	CPBL	ICD	–	Blanking clamp pulses	When the input is High, BCP1 (pin 37) and BCP2 (pin 36) are Low.
37	BCP1	**o**	⎍	Optical black clamp pulse 1	A pulse to clamp the optical black signal. This pulse is continuous at Horizontal cycle when CPMD (Pin 25) and CPBL (pin 36) are Low.hen CPMD is High and PBL is Low, output stays Low during the absence of effective pixels within the Vertical blanking, otherwise is continuous at Horizontal cycle.
38	BCP2	**o**	⎍	Optical black clamp pulse 2	BCP2 is the same as BCP1 (pin 37) except that BCP2 is delayed by 700 ns from BCP 1
39	PBLK	**o**	⎍ or ⎎	Pre-blanking pulse	Equivalent to CBLK (pin 16) pulse except for shorter pulse width with cut-off falling edge. When CKCH (pin 22) is L level, the polarity is positive. When CKCH is H level, the polarity is negative.
40	ID	**o**	**n**	Line index pulse	The pulse is used in color separator. The signal switches between H and L at every line. It resets at the 273th I ine when in NTSC mode, and at the 326th line when in PAL mode.
41	NC	–	–	No connection	A pin for no use.
42	WBLK	**o**	⎍ or ⎎	Wide blanking pulse	Equivalent to CBLK (pin 16) except that its pulse width is wider than that of CBLK. When CKCH (pin 22) is L level, the polarity is positive, When CKCH is H level, the polarity is negative.
43	NC	–	–	No connection	A pin for no use.
44	SCOF	ICD	–	Subcarrier control	An input pin for controlling SC1 (pin 4), SC2 (pin 5) at NTSC mode. When SCOF is L level, SC 1 and SC2 are recurred. When SCOF is H level, SC 1 and SC2 are held at L level.

IC : Input pin (CMOS level).
ICU : Input pin (CMOS level with pull-up resistor).
ICD : Input pin (CMOS level with pull-down resistor).
ICSU : Schmitt-trigger input pin (CMOS level with pull-up resistor)
o : Output pin.
TO : Tri-state output pin,

TIMING DAIGRAM

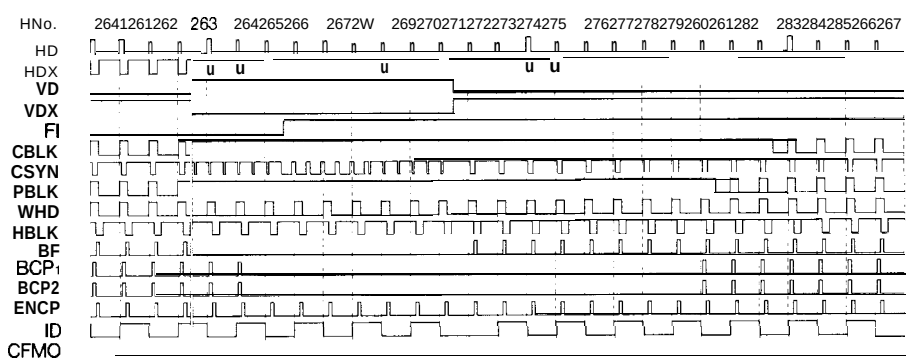
VERTICAL PULSE <NTSC, CKCH = L>

(ODD FIELD)



* CPMD = H, CPBL = L

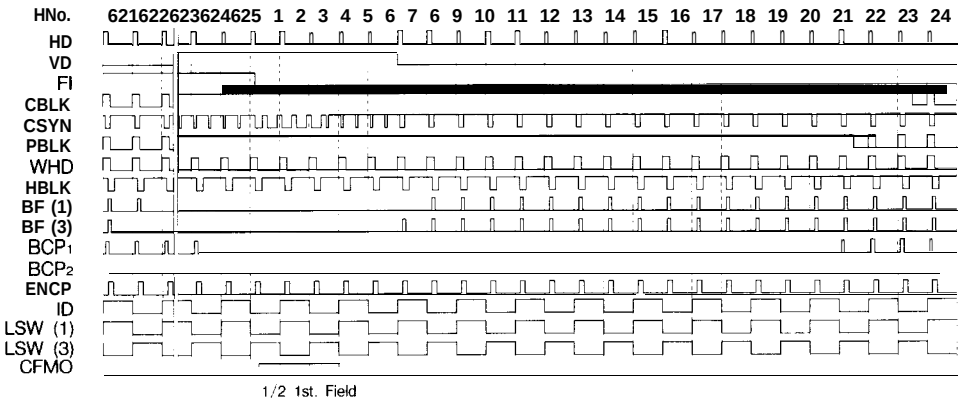
(EVEN FIELD)



* CPMD = H, CPBL = L

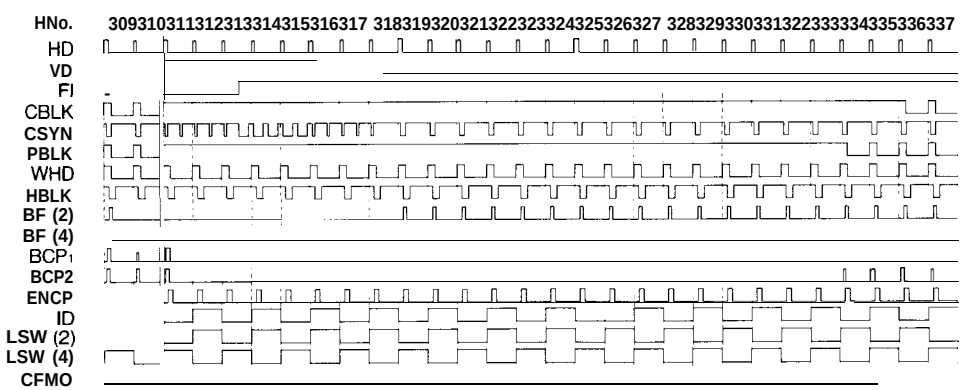
VERTICAL PULSE < PAL, CKCH=L >

(1st, 3rd FIELD)



* CPMD = H, **CPBL=L**

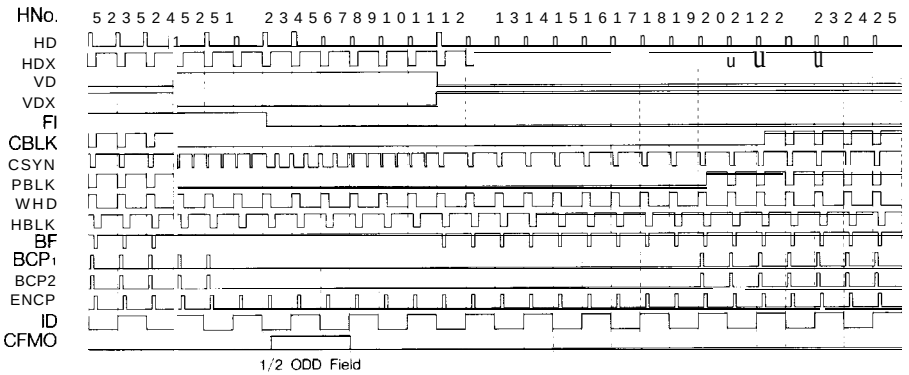
(2nd, 4th FIELD)



* CPMD = H, **CPBL=L**

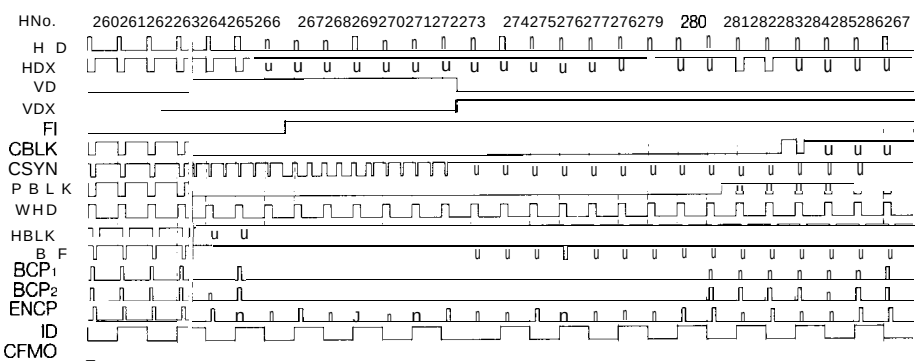
VERTICAL PULSE <NTSC, CKCH=H>

(ODD FIELD)



*CPMD=H, CPBL=L

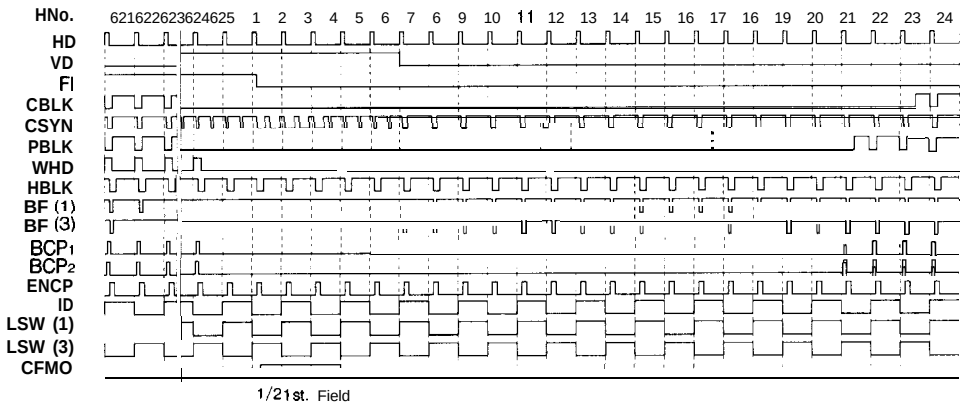
(EVEN FIELD)



*CPMD=H, CPBL=L

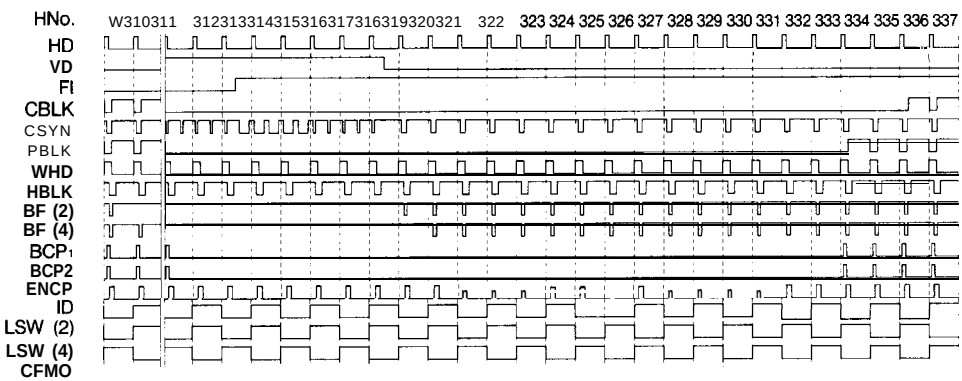
VERTICAL PULSE < PAL, CKCH=H>

(1st, 3rd FIELD)



∗CPMD = H, CPBL = L

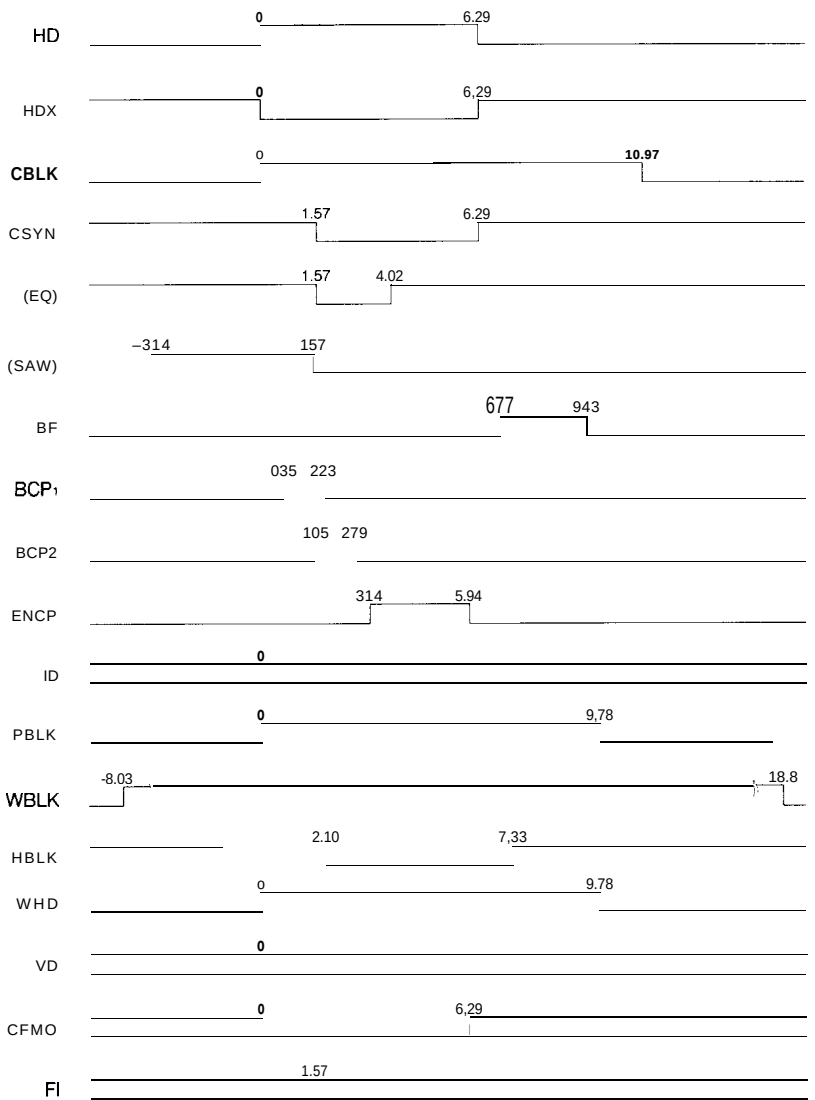
(2nd, 4th FIELD)



∗CPMD = H, CPBL = L

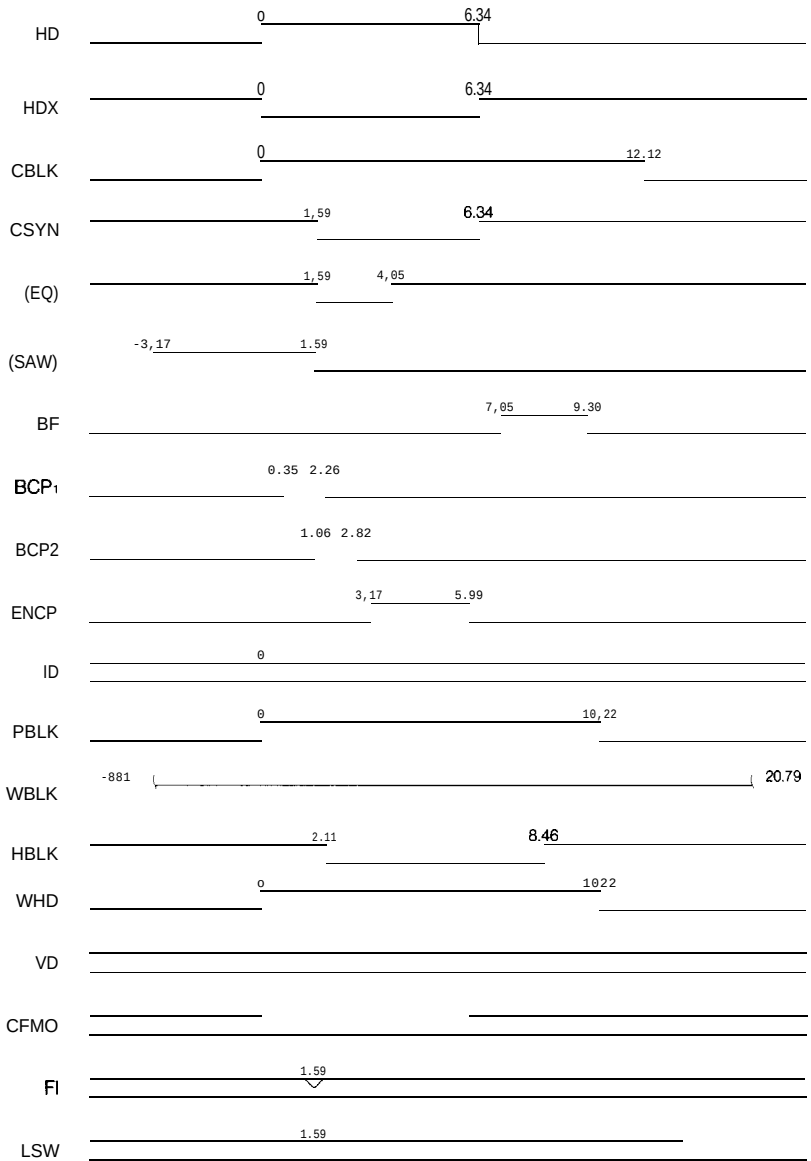
HORIZONTAL PULSE < NTSC, CKCH = L >

Unit : μs



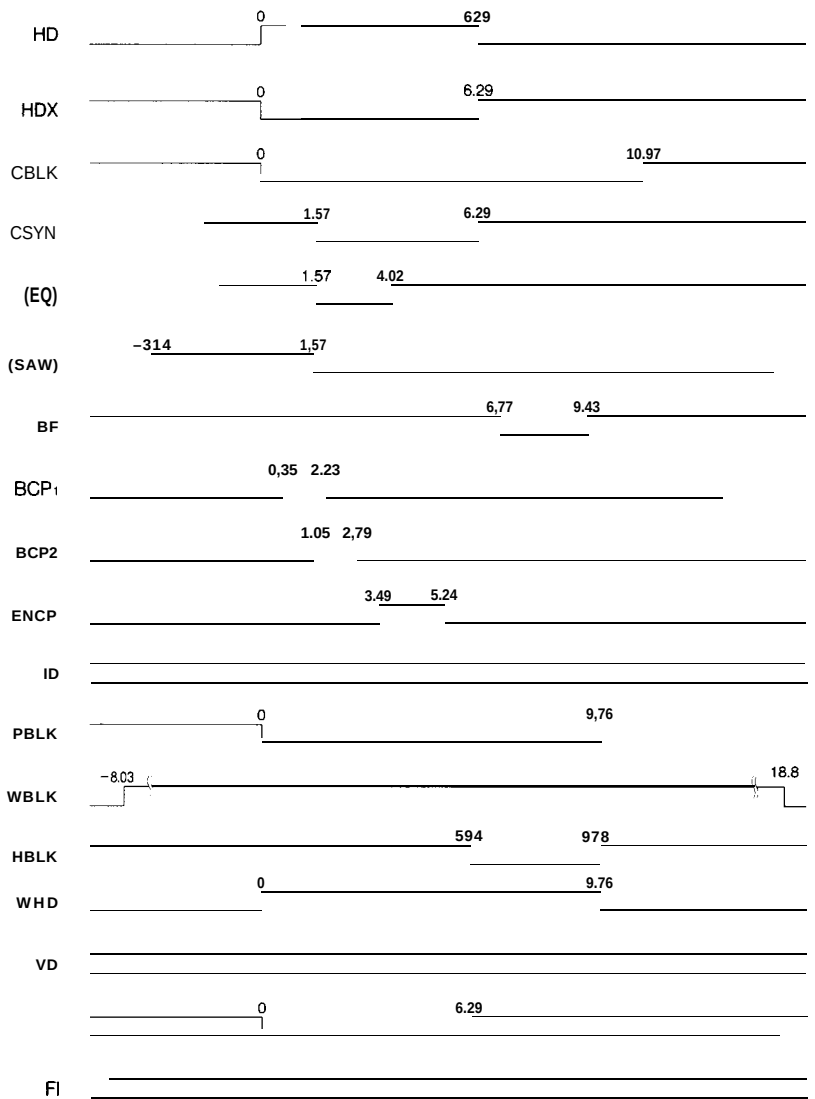
HORIZONTAL PULSE < PAL, CKCH = L >

Unit : μs



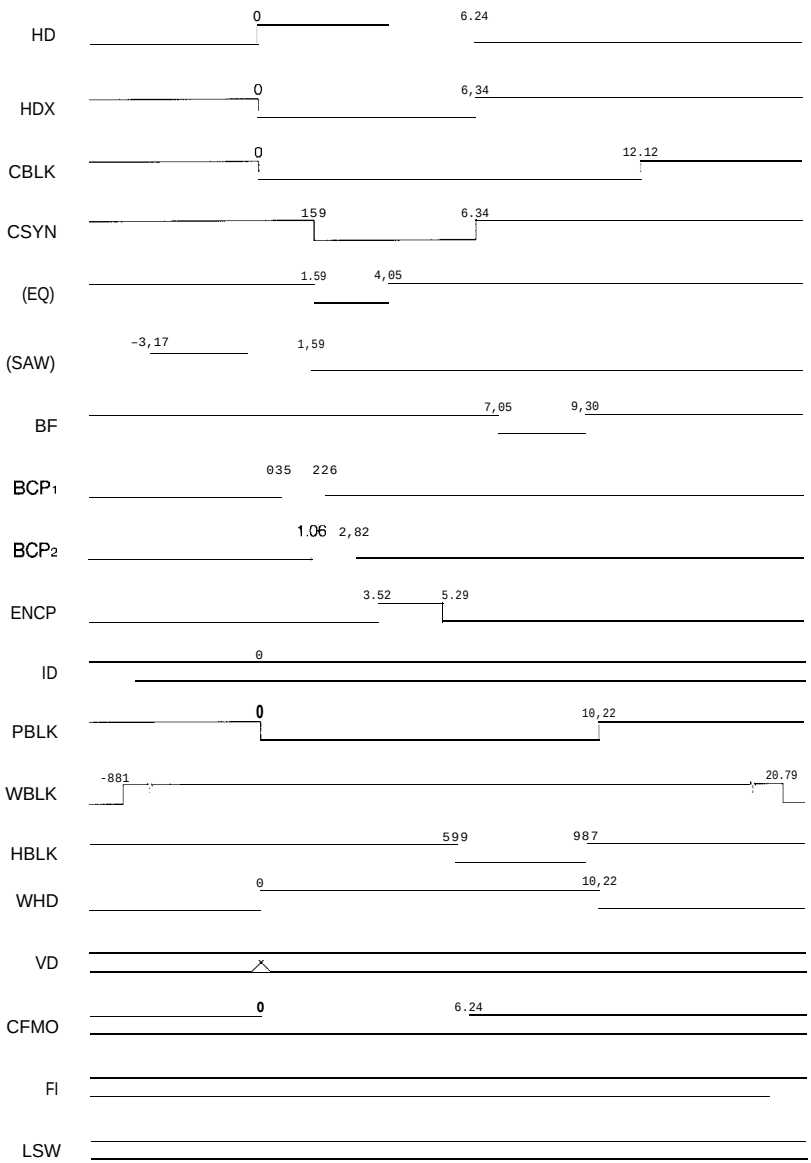
HORIZONTAL PULSE < NTSC, CKCH=H >

Unit : μS



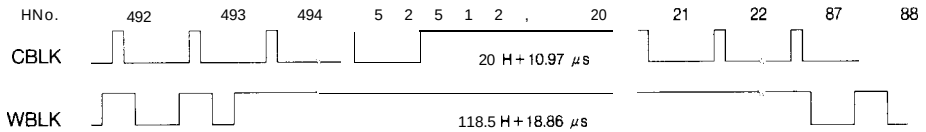
HORIZONTAL PULSE < PAL, CKCH=H>

Unit : μs

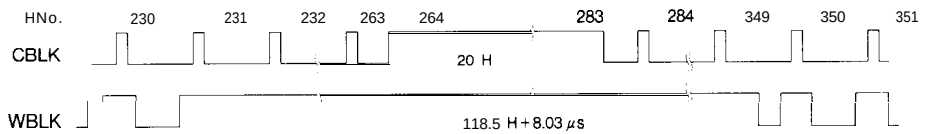


"WBLK" PULSE <CKCH=L>

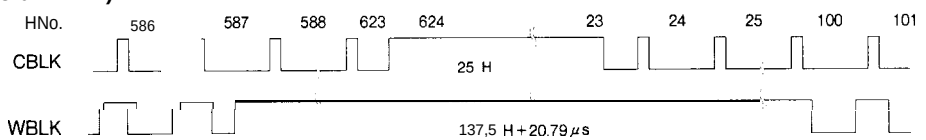
NTSC : (ODD FIELD)



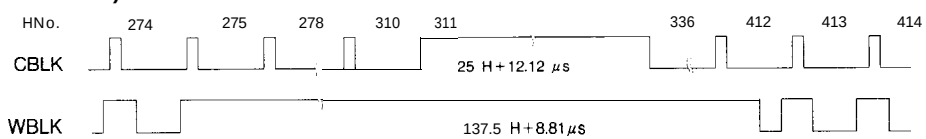
(EVEN FIELD)



PAL : (1st, 3rd FIELD)

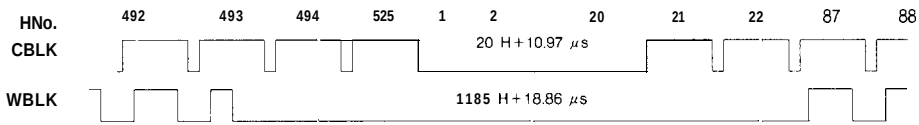


(2nd, 4th FIELD)

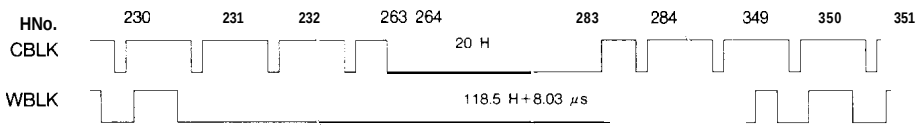


"WBLK" PULSE < CKCH=H>

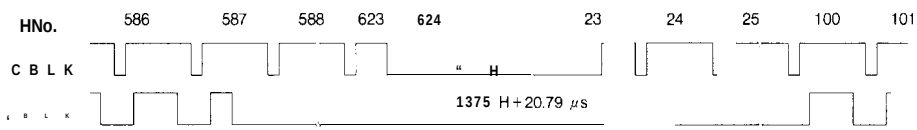
NTSC : (ODD FIELD)



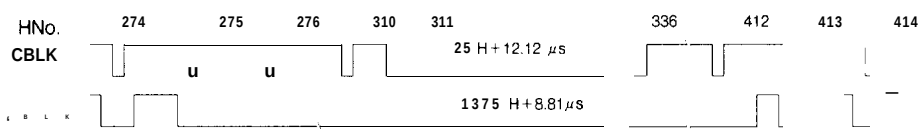
(EVEN FIELD)



PAL : (1st, 3rd FIELD)

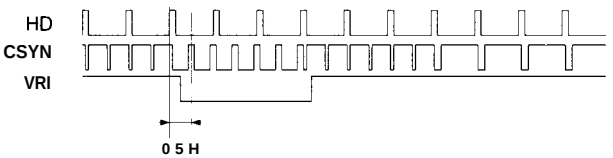


(2nd, 4th FIELD)

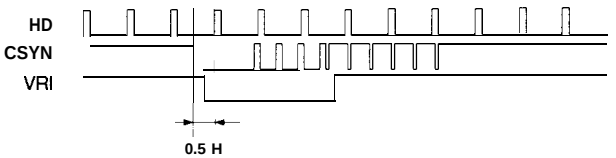


"VRI" INPUT TIMING

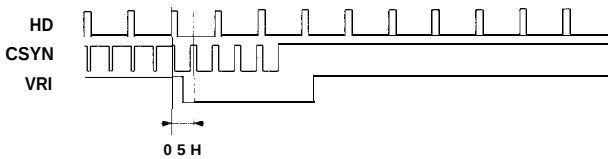
NTSC : (ODD FIELD)



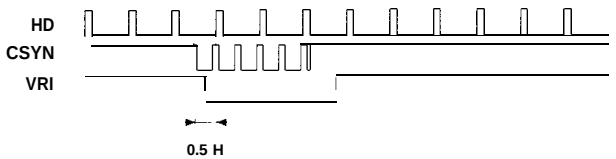
(EVEN FIELD)



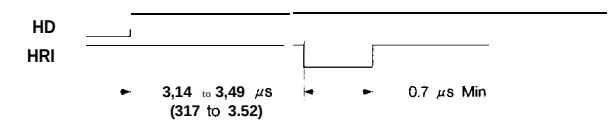
PAL : (1st, 3rd FIELD)



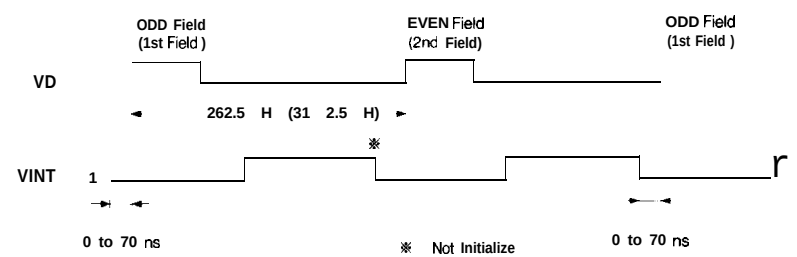
(2nd, 4th FIELD)



"HRI" INPUT TIMING ( ): PAL



"VINT" INPUT TIMING ( ): PAL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	− 0.3 to +7.0	v
Input voltage	VI	−0.3 to V_{CC} +0.3	v
Output voltage	Vo	−0.3 to V_{CC} +0.3	v
Operation temperature	Topr	−20 to +70	°c
Storage temperature	Tstg	−55 to +150	°c

DC CHARACTERISTICS

(V_{CC} = +5 V ± 10%, Ta=−20 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input Low voltage	V_{IL}				1,5	v	t
Input High voltage	V_{IH}		3.5			v	
Input Low current	$\|I_{IL1}\|$	VI=0 v			1.0	μA	2
	$\|I_{IL2}\|$	VI=0 v	8.0		60	μA	3
Input High current	$\|I_{IH1}\|$	VI= V_{CC}			1.0	μA	4
	$\|I_{IH2}\|$	VI =V_{CC}	8.0		60	μA	5
Output High voltage	V_{OH1}	I_{OH} = −2 mA	4.0			v	6
Output Low voltage	V_{OL1}	I_{OL} = 4 mA			0.4	v	
Output High voltage	V_{OH2}	I_{OH} = −3 mA	4.0			v	7
Output Low voltage	V_{OL2}	I_{OL} = 4 mA			0.4	v	
Output High voltage	V_{OH3}	I_{OH} = −4 mA	4.0			v	8
Output Low voltage	V_{OL3}	I_{OL} = 8 mA			0.4	v	
Output High voltage	V_{OH4}	I_{OH} = −8 mA	4,0			v	9
Output Low voltage	V_{OL4}	I_{OL} = 8 mA			0.4	v	
Output High voltage	V_{OH5}	I_{OH} = −8 mA	4.0			v	10
Output Low voltage	V_{OL5}	I_{OL} = 16 mA			0.4	v	

NOTES :

1. Applied to inputs (IC, ICD, ICU, OSCI).
2. Applied to inputs (IC, ICD, OSCI).
3. Applied to input (ICD).
4. Applied to inputs (IC, ICU, OSCI).
5. Applied to input (ICD).
6. Applied to outputs (O, OR1, OSC0).
7. Applied to output (OR1 A).
8. Applied to output (ORI B).
9. Applied to output (OR1 C).
10. Applied to output (OR1 D).

PIN FUNCTION

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
1	CKI	OscI	⎍	Clock input	An input pin for reference clock oscillation. The frequencies are as follows : At NTSC mode : 28.63636 MHz (1820 fH) At PAL mode : 28.37500 MHz (1816 fH) (fH=Horizontal frequency)
2	CKO	Osco	–	Clock output	An input pin for reference clock oscillation. The output is the inverse CKI (pin 1).
3	TRIG	ICU	–	Trigger input	An input pin to directly control the shutter speed. For details, see shutter control,
4	EDo	ICU	–	Shutter speed switching input O	An input pin to control the shutter speed. For details, see shutter control.
5	ED_1	ICU	–	Shutter speed switching input 1	An input pin to control the shutter speed. For details, see shutter control.
6	ED2	ICU	–	Shutter speed switching input 2	An input pin to control the shutter speed. For details, see shutter control.
7	GND	–	–	Ground	A grounding pin.
8	SMDI	ICU	–	Shutter mode select input 1	An input pin to Select Shutter mode. For details, see shutter control.
9	SMD2	ICU	–	Shutter mode select input 2	An input pin to Select Shutter mode. For details, see shutter control,
10	MRI	ICU	–	FR phase control input 1	Pins to control the phase between the rising edge of FHI (pin 17) and FR (pin 12).
11	MR2	ICU	–	FR phase control input 2	
12	FR	ORIC	⎍	Reset pulse	A reset pulse for CCD. Correct to ϕ_R of CCD through the DC offset circuit.
13	MCI	ICU	–	FCX phase control input 1	Pins to control the phase betwean the falling edge of FH_1 (pin 17) and FCX (pin 32).
14	MC2	ICU	–	FCX phase control input 2	
15	LH_1	ORIA	⎍	Last horizontal transfer pulse	A horizontal transfer pulse for last gate of CCD. Connect to ϕ_{LH1} of CCD without inversing driver.
16	Vcc	–	–	Power supply	Supply +5 V power.
17	FH_1	ORI D	⎍	Horizontal transfer pulse 1	A horizontal transfer pulse for CCD. Connect to ϕ_{HI} of CCD without inversing driver.
18	FH2	ORI D	⎍	Horizontal transfer pulse 2	A horizontal transfer pulse for CCD. Connect to ϕ_{H2} of CCD without inversing driver.

MR_1	H	L	L	H
MR_2	H	H	L	L
Pulse width	A	$A+\alpha$	$A+2\alpha$	$A+3\alpha$

MC_1	H	L	L	H
MC_2	H	H	L	L
Phase difference	A	$A+\alpha$	$A+2\alpha$	$A+3\alpha$

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
19	GND	–	–	Ground	A grounding pin.
20	MS_1	ICU	–	FSX phase control input 1	Pins to control the phase between the rising edge of FHI (pin 17) and the falling edge of FSX (pin 33).
21	MS2	ICU	–	FSX phase control input 2	
22	OFDX	o	⊓	OFD pulse output	A pulse that sweeps the charge of the photodiode for electrical shutter. It is held at H level in Normal mode.
23	VI x	o	⊓	Vertical transfer pulse 1	A vertical transfer pulse for CCD. Connect to the 1A pin of the LR36683N V driver LSI.
24	V_{HIX}	o	⊓	Read out pulse 1	A pulse that transfers the charge of the photodiode to the vertical shift register, Connect to the 1 B pin of the LR36663N V driver LSI.
25	V2X	o	J-L	Vertical transfer pulse 2	A vertical transfer pulse for CCD. Connect to the 2A pin of the LR36683N V driver LSI.
26	V3X	o	V	Vertical transfer pulse 3	A vertical transfer pulse for CCD. Connect to the 3A pin of the LR36683N V driver LSI.
27	VH3X	o	⊓	Read out pulse 2	A pulse that transfers the charge of the photodiode to the vertical shift register. Connect to the 3B pin of the LR36663N V driver LSI.
28	V4X	o	⊓	Vertical transfer pulse 4	A vertical transfer pulse for CCD. Connect to the 4A pin of the LR36683N V driver LSI.
29	CNTV	ICU	–	Read out pulse control input	An input pin to control VH_{1X} (pin 21), VH3X (pin 27). H level or open : Normal VH_{IX} and VH_{2X}. L level : VH_{IX} and VH2X are held at High level.
30	V_{CC}	–	–	Power supply	Supply +5 V power.
31	GND	–	–	Ground	A grounding pin.
32	FCX	ORI B	⊓	CDS pulse 1	A pulse to clamp the feed through level from CCD.
33	FSX	ORIB	⊓	CDS pulse 2	A pulse to sample-hold the signal from CCD.
34	SP_{1X}	ORI	⊓	Color sampling pulse 1	A pin to output the color sampling pulse for color demodulation based upon the output signal from CCD.
35	SP_{2X}	OR I	V	Color sampling pulse 2	A pin to output the color sampling pulse for color demodulation based upon the output signal from CCD.
36	D_{SIX}	ORI	⊓	Pulse output 1	A pin to output the driving pulse (DL1 X) for CCD line and the sampling pulse (SHI). These are changed with SLCT (pin 47).
37	DS2X	OR 1	⊓	Pulse output 2	A pin to output the driving pulse (DL2X) for CCD delay line and the sampling pulse (DH2). These are changed with SLCT (pin 47).

MS_1	H	L	L	H
MS_2	H	H	L	L
Phase difference	A	$A+\alpha$	$A+2\alpha$	$A+3\alpha$

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
38	MPI	ICU	–	SP_{1X}, SP2X phase control input 1	Pins to control the phase between the rising edge of FH_1 (pin 17) and the falling edge of SP_{1X} (pin 34) and SP2X (pin 35).
39	CLP	o	n	Clamp pulse	A pulse to clamp the dummy outputs of CCD.
40	MP2	ICU	–	SPIX, SP2X phase control input 2	Pins to control the phase between the rising edge of FHI (pin 17) and the falling edge of SP_{1X} (pin 34) and SP2X (pin 35).
41	CLK	OR1	⎍	1/2 dividing	The frequency is 1/2 dividing pulse of a reference clock CKI (pin 1). Connect to clock input terminal of SSG LSI. At NTSC mode : 14.31818 MHz (910 fH) At PAL mode : 14.18750 MHz (908 fH)
42	PSMD	ICU	–	Shutter mode select input 3	An input pin to select shutter speed data. H level or open : Pararell Data Input mode, L level : Serial Data Input mode.
43	HD	IC	n	Horizonal reference	An input pin for the horizontal reference signal. Connect to HD pin of SSG LSI.
44	VD	IC	⎍	Vertical reference	An input pin for the vertical reference signal. Connect to VD pin of SSG LSI.
45	TVMD	ICU	–	TV mode select	An input pin to select TV standards. L level : NTSC mode. H level or open : PAL mode,
48	PWMD	ICU	–	Power save input	An input pin for Power Save mode, H level or open : All output pulses are occurred. L level : CLK (pin 41) output is occurred.
47	SLCT	ICU	–	Pulse select input	An input for switching DSI x and DS2X H level or open : DLI x and DL2x L level : SH 1 and SH2.
48	TEST	ICD	–	Test pin	A test pin. Set open or to L level in the Normal mode,

IC	: Input pin (CMOS level).
ICU	: Input pin (CMOS level with pull up resistor).
ICD	: Input pin (CMOS level with pull down resistor).
O, ORI, ORIA, ORIB, ORIC, ORID	: Output pin.
Oscl	: Input pin for oscillation.
Osco	: Output pin for oscillation.

MP1	H	L	L	H
MP2	H	H	L	L
Phase difference	A	A+ α	A+2 α	A+3 α

NOTES :

Shutter Speed Control

Shutter mode

TRIG	SMD1	SMD2	SHUTTER MODE	DESCRIPTION
–	H	x	Normal mode	This mode is Normal Shutter mode. 1/60 s at NTSC mode, 1/50 s at PAL mode
–	L	L	Flicker-less Shutter mode	Flicker-less mode. 1/100 s at NTSC mode, 1/120 s at PAL mode.
H	H	H	High Speed Shutter mode	This mode is higher shutter speed than Normal mode.
↓	L	x	External Shutter mode	This mode is effective at High Spaed Shutter mode. OFDX pulse is held at H level after TRIG input is "Low". Whenever TRIG input is "Low" the shutter is stopped at Flicker-less Shutter mode or High Speed Shutter **mode.** **It is necessary with** EDo= ED1 = ED2= L (1/1 0000 s) for wide variable shutter speed.

Input format of shutter speed control date

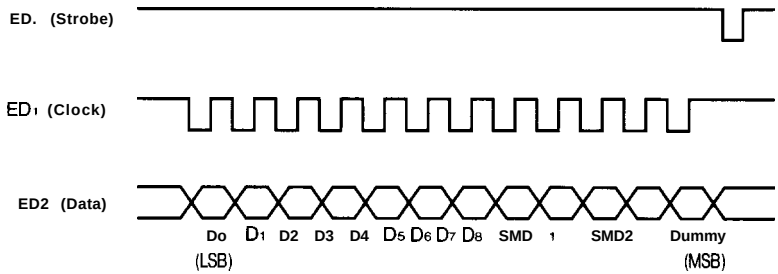
PSMD	INPUT FORMAT	DESCRIPTION
H	Pararell data input	There are 8-shutter speed. 1 /60 (NTSC), 1 /50 (PAL), 1/1 25, 1 /250, 1 /500, 1/1 000, 1/2 000, 1/4000, 1/10 000
L	Serial data input	It is possible to switching per 1 H period. EDo = **strobe,** ED I = clock, ED2 = data

Pararell data input

MODE	TVMD	PSMD	SMD1	SMD2	EDo	ED1	ED2	SHUTTER SPEED (a)
Normal mode	L	x	H	x	x	x	x	1 /60
	H	x	H	x	x	x	x	1 /50
Flicker-less mode	L	x	L	L	x	x	x	1/100
	H	x	L	L	x	x	x	1/120
High Speed Shutter **mode**	L	H	L	H	H	H	H	1 /60
	H	H	L	H	H	H	H	1 /50
	x	H	L	H	L	H	H	1/125
	x	H	L	H	H	L	H	1 /250
	x	H	L	H	L	L	H	1 /500
	x	H	L	H	H	H	L	1/1 000
	x	H	L	H	L	H	L	1/2 000
	x	H	L	H	H	L	L	1/4 000
	x	H	L	H	L	L	L	1/10000

X = H **or** L

Serial data input



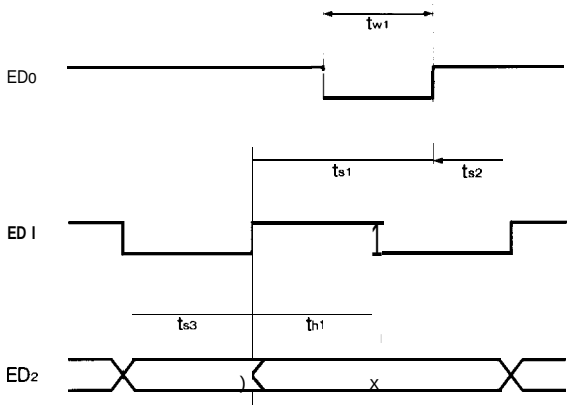
The calculate method of shutter speed,
NTSC : T= 1 / (n – 249) x 63.56+25.28 [μs] (250≤n≤509)
PAL : T= 1 / (n – 299) x 64.00+25.52 [μs] (200≤n≤509)

Shutter speed table

VMD (Pin 45)	SMD1 (Pin 8)	SMD2 (Pin 9)	PSMD [Fin 42]	SERIAL DATA Do	D1	D2	D3	D4	D5	D6	D7	D8	SMD1	SMD2	HEX	SHUTTER SPEED (s)	CALCULATION (s)
L	x	x	L	L	H	L	H	H	H	H	H	L	L	H	4FA	1/10000	1/1 1256
				L	L	H	H	H	H	H	H	L	L	H	4FC	1/4 000	1/4 630
				L	L	L	L	L	L	L	L	H	L	H	500	1/2 000	1/2127
				L	L	L	H	L	L	L	L	H	L	H	508	1/1 000	1/1 022
				L	L	L	H	H	L	L	L	H	L	H	518	1 /500	1 /501
				H	H	H	L	H	H	L	L	H	L	H	537	1 /250	1 /252
				L	H	H	L	H	H	H	L	H	L	H	576	1/125	1/125
				L	H	H	L	H	L	L	H	H	L	H	596	1/100	1/100
				H	L	H	H	H	H	H	H	H	L	H	5FD	1 /60	1 /60
H	x	x	L	L	L	L	H	L	L	H	H	L	L	H	4C8	1/10000	1/11 171
				L	H	L	H	L	L	H	H	L	L	H	4CA	1/4 000	1/4 597
				L	H	H	H	L	L	H	H	L	L	H	4CE	1/2 000	1/2112
				L	H	H	L	H	L	H	H	L	L	H	4D6	1/1 000	1/1 015
				L	H	H	L	L	H	H	H	L	L	H	4E6	1 /500	1 /498
				H	L	H	L	L	L	L	L	H	L	H	505	1 /250	1 /250
				H	H	L	L	L	L	H	L	H	L	H	543	1/125	1/125
				H	L	L	H	L	L	H	L	H	L	H	549	1/120	1/120
				H	L	H	H	H	H	H	H	H	L	H	5FD	1 /50	1 /50
L	x	x	L	x	x	x	x	x	x	x	x	x	L	L	–	1/100	1/100
H	x	x	L	x	x	x	x	x	x	x	x	x	L	L	–	1/120	1/120
L	x	x	L	x	x	x	x	x	x	x	x	x	H	H	–	1 /60	1 /60
H	x	x	L	x	x	x	x	x	x	x	x	x	H	H	–	1 /50	1 /50

X=H or L

AC Electrical Characteristics of Input Serial Data



SYMBOL	CONDITIONS	MIN.	MAX.
t_{w1}	EDo pulse width L	20 ns	50 μs
t_{s1}	Setup time ED_1 to EDo	20 ns	–
t_{s2}	Setup time EDI to EDo	20 ns	–
t_{s3}	Setup time ED_1 to ED2	20 ns	–
t_{h1}	Hold time ED_1 to ED2	20 ns	-